Serial Peripheral Interface (SPI)

SPI Features (1/2)

- Full duplex synchronous transfers on 3 lines
- Simplex synchronous transfers on 2 lines with or without a bi-directional data line
- Programmable data order with MSB-first or LSB-first shifting
- Master or slave operation
- Baud rate up to SYSCLK/2: (8MHz)
- Programmable clock polarity and phase
- NSS management by hardware or software for both master and slave: Dynamic change of Master/Slave operations

SPI Features (2/2)

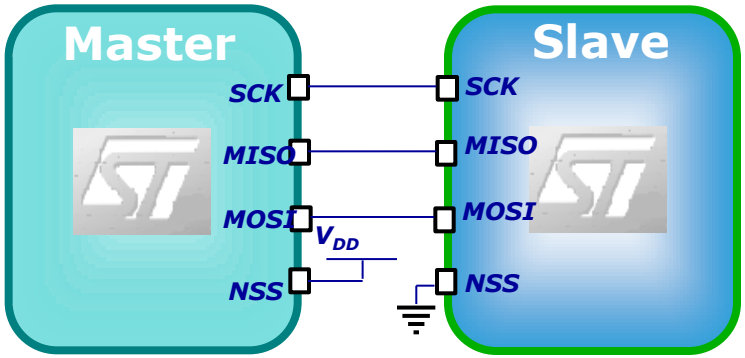
- Dedicated transmission and reception flags (Tx buffer Empty and Rx buffer Not Empty) with interrupt capability
- SPI bus busy status flag
- Master mode fault and overrun flags with interrupt capability
- Hardware CRC feature for reliable communication
- Wake-up capability from low power mode
- Support for DMA (15x devices only)

DMA Capability on 15x devices

- The SPI has a DMA Tx and Rx requests
- The SPI requests is mapped on a different DMA channel: possibility to use DMA for both SPI transfer direction in the same time
- Calculated CRC value is automatically transmitted at the end of data transfer

Full Duplex Communication

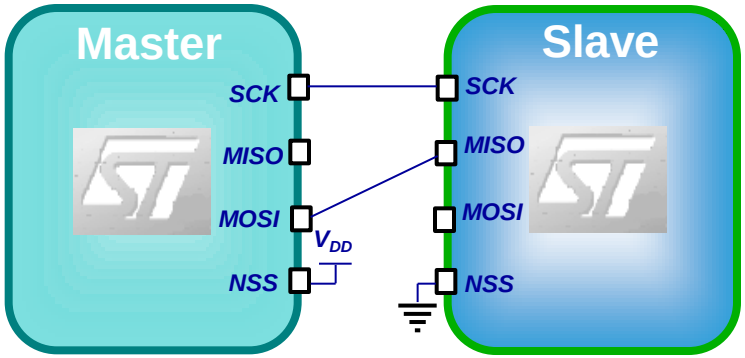
- SPI supports Full duplex and Rx-Only communication mode :
  - Full-duplex, three-wire synchronous transfer



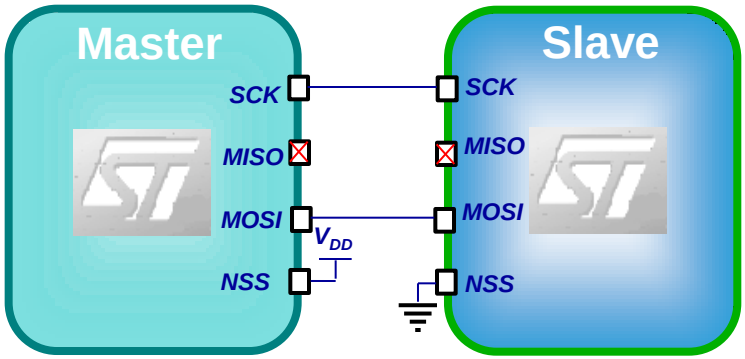
Full Duplex

Simplex Communication

- SPI supports simplex communication mode:
  - Bidirectional: 1 Clock and 1 bi-directional data wire (One bit direction transfer control)
  - Rx-Only: 1 Clock and 1 unidirectional data wire

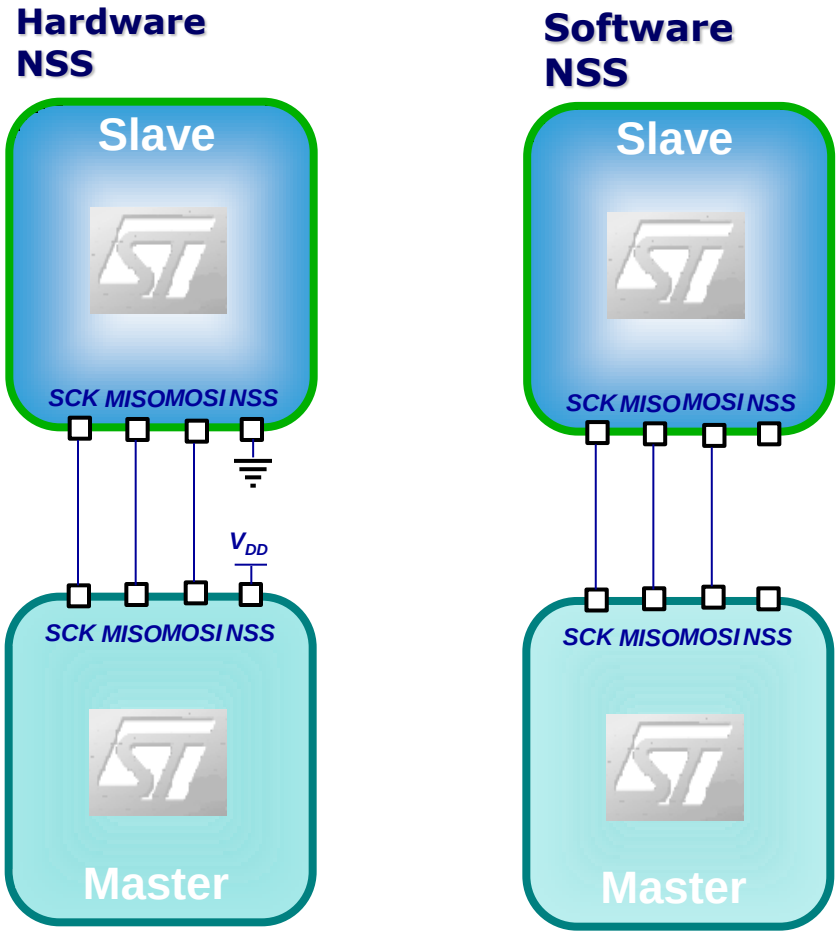


Bi-directional



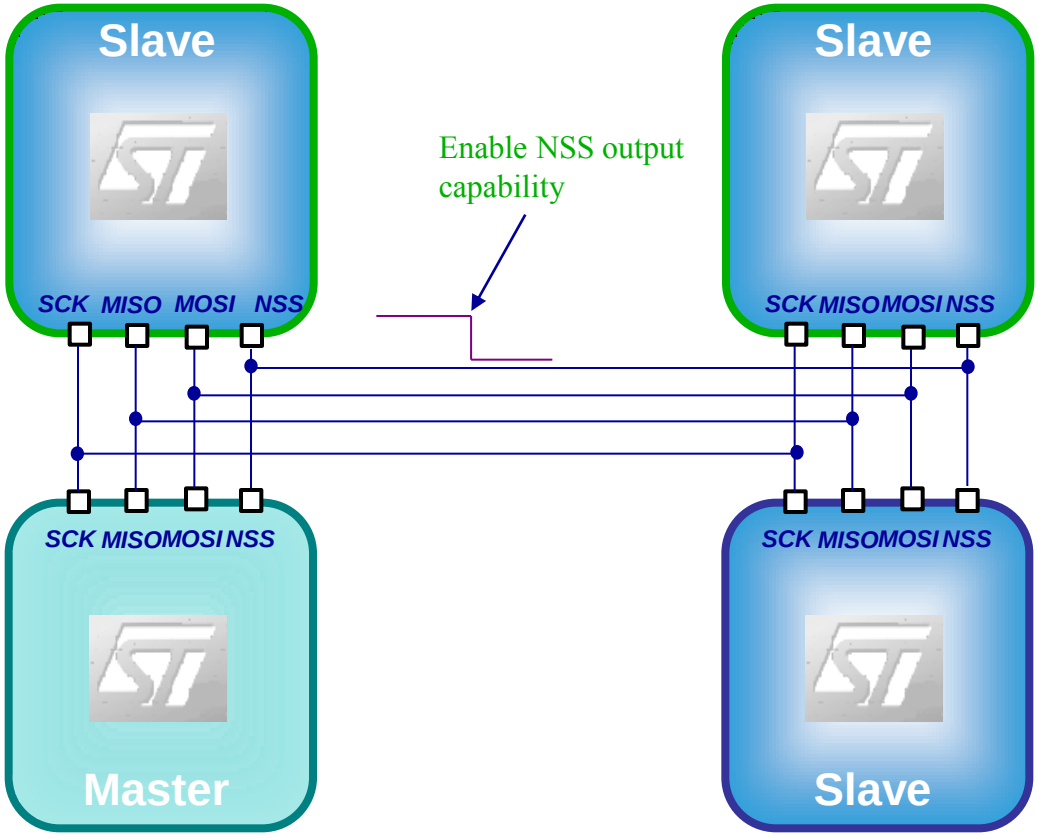
Rx Only
(Slave)

NSS Hardware & Software Management



- Both Master and Slave NSS pins could be used for other purpose
- Provides the possibility of dynamic change of Master/Slave operations: No hardware limitation to switch from master to slave or slave to master in the same application

Single Master: Slave Select output Management



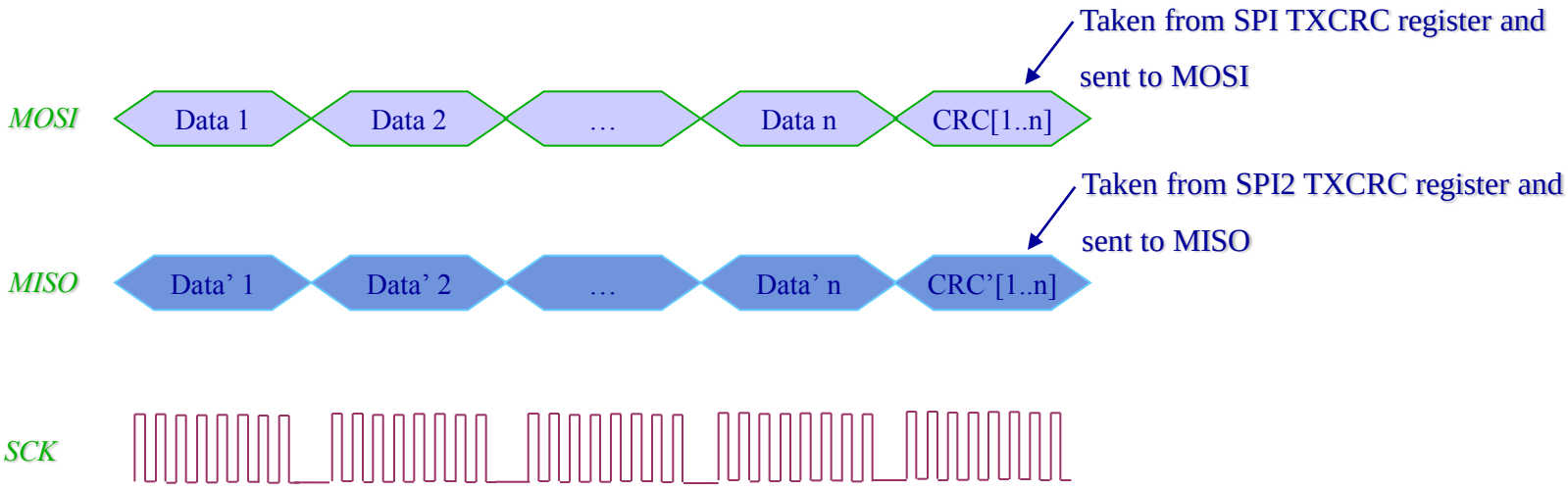
- Each device can be a unique master by enabling its NSS as output and driving it low: all other devices became slaves.
- No need for external GPIO pin to drive slaves NSS pins

CRC Calculation (1/2)

- Hardware CRC feature for reliable communication (only for Full Duplex mode) :
  - Separate CRC calculators implemented for transmitted and received data
  - CRC value can be transmitted as last byte in transmission mode
  - CRC error checking for last received byte and interrupt generation on error
  - Programmable CRC polynomial calculation
  - CRC calculation based on:
    - CRC8 for 8-bit data
    - CRC16-CCITT standard for 16-bit data

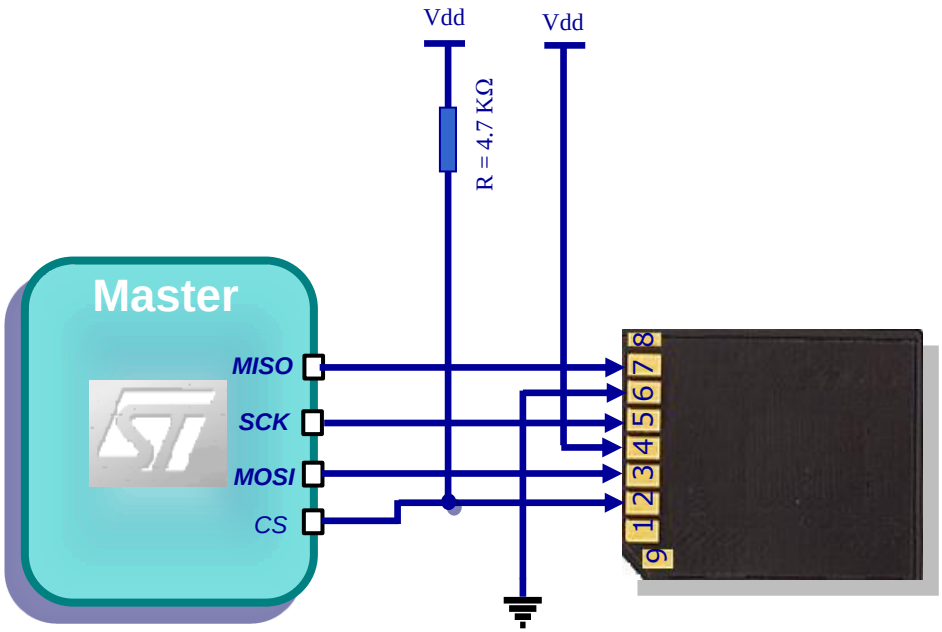
CRC Calculation (2/2)

- Example of n data transfer between two SPIs followed by the CRC transmission of each one in Full-duplex mode



Basic SD/MMC support SPI protocol:

- Performance: speed up to 8MHz
- Error checking: hardware CRC calculation



Communication and Error Management

- Communication management
  - Transmission buffer empty (IT)
  - Receive buffer full (IT)
  - Busy flag
  - Wake-up flag (IT)
  - DMA

- Error Management
  - Overrun condition
    - OVR bit is set if a new data is received but the previous one has not been read
  - Master Mode fault
    - MODF bit is set if the device is the master and NSS pin (or SSI bit if SSM is set) goes low. The SPI cell then is automatically deactivated
  - CRC error
    - If CRC is enabled, CRCERR bit is set whenever the received CRC does not match the one calculated.

Quiz

- What is the maximum speed of the STM8L SPI?

  _____

- What are the DMA requests supported by the SPI?

  _____

- How to reduce as much as possible the number of pins used by the SPI of the STM8L?

  _____

- What happens if the NSS pin goes to zero while the device is configured in master mode?

  _____

- What are the different error flags?

  _____

CONFIDENTIALITY OBLIGATIONS:

THIS DOCUMENT CONTAINS SENSITIVE INFORMATION.

IT IS CLASSIFIED “MICROCONTROLLERS, MEMORIES & SECURE MCUs (MMS) RESTRICTED AND ITS DISTRIBUTION IS SUBMITTED TO ST/MMS AUTHORIZATION

AT ALL TIMES YOU SHOULD COMPLY WITH THE FOLLOWING SECURITY RULES:

- DO NOT COPY OR REPRODUCE ALL OR PART OF THIS DOCUMENT
- KEEP THIS DOCUMENT LOCKED AWAY
- FURTHER COPIES CAN BE PROVIDED ON A “NEED TO KNOW BASIS”, PLEASE CONTACT YOUR LOCAL ST SALES OFFICE OR DOCUMENT WRITTER.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2015 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

www.st.com

life.augmented